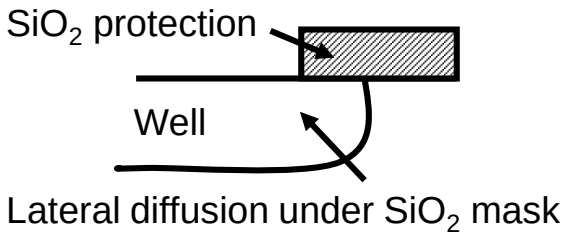
Component Matching Issues

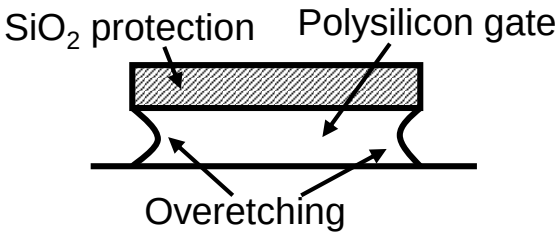
Component Matching Issues

- Effective component sizes differ from mask sizes

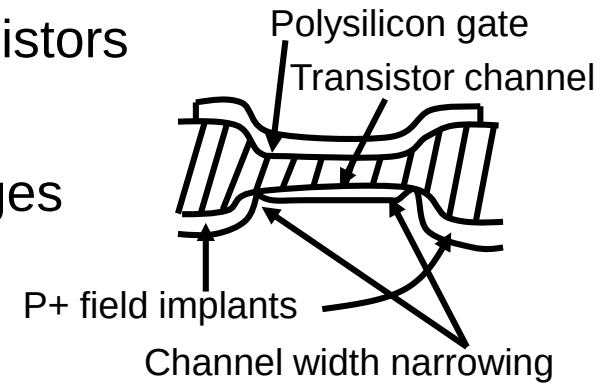
- Examples
  - Lateral diffusion due to
    - Ion implantation
    - Annealing



  - Overetching



  - Narrow channel effect
    - High doping density at the sides of transistors
      - Due to channel stop implantation
    - Decrease channel charge density at edges
    - Decrease effective channel width

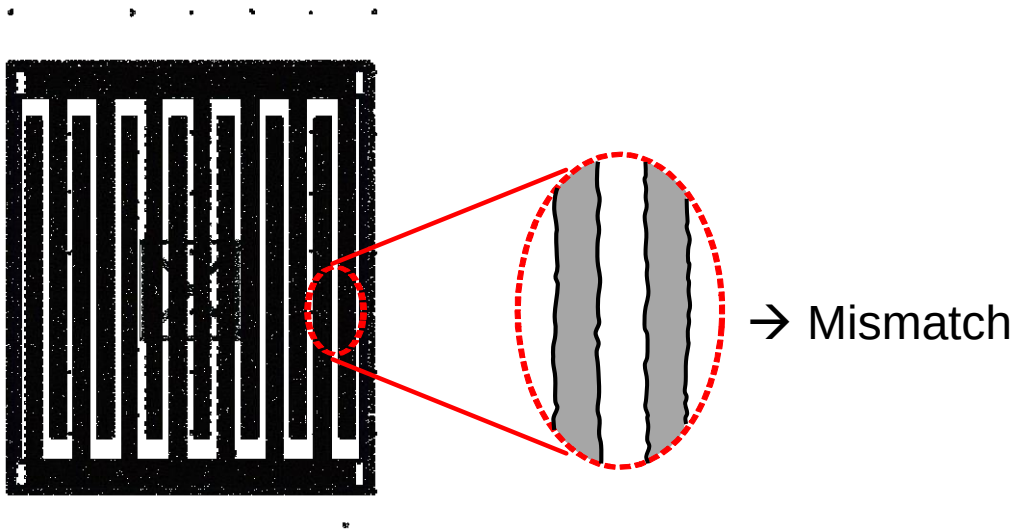


Component Matching Issues (Cont.)

- Absolute component sizes can seldom be accurately determined. The inaccuracies also affect the ratio of sizes (with a lesser degree) when the ratio is not unity.

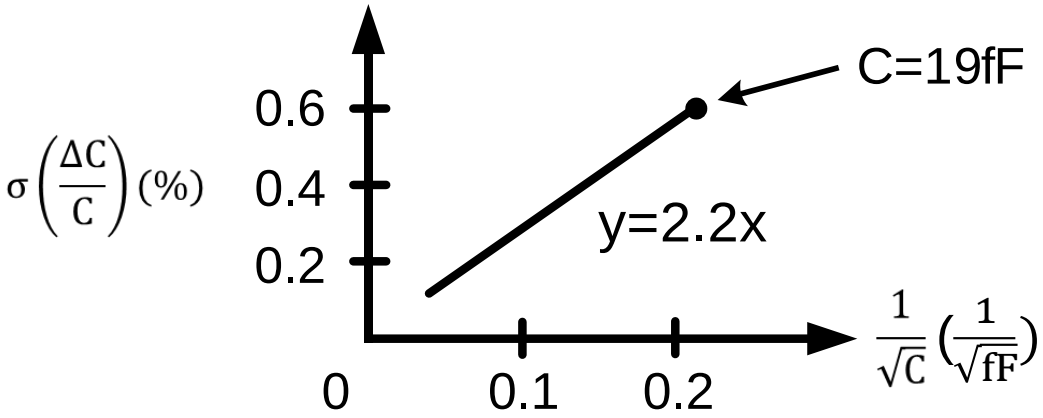
- Matching second-order size error effects is done mainly by making larger objects out of several unit-sized components connected together. Also, for best ratio accuracy, the boundary conditions around all objects should be matched, even when this means adding extra unused components. (Examples given later)

- Mismatch profile
  - Random mismatch
  - Gradient mismatch



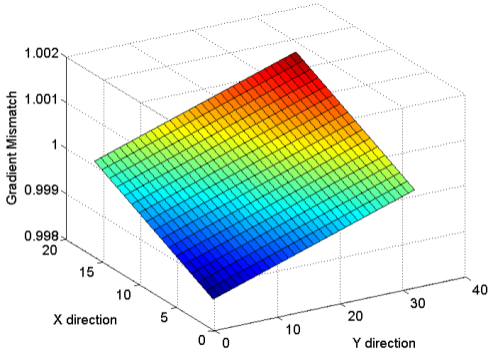
Component Matching Issues (Cont.)

- Random mismatch: Larger capacitance area → Smaller mismatch (%)

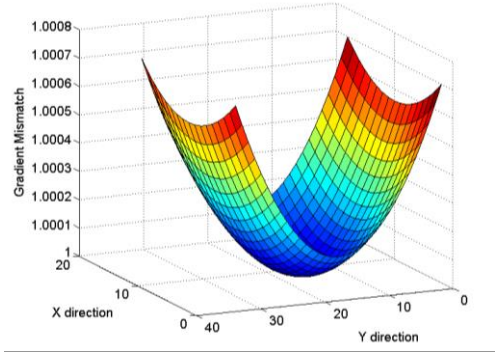


- Gradient mismatch: Larger capacitance spacing → Larger mismatch (%)

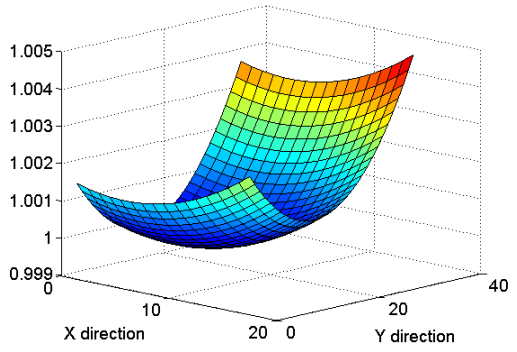
1st order
Gradient mismatch model



2nd order
Gradient mismatch model

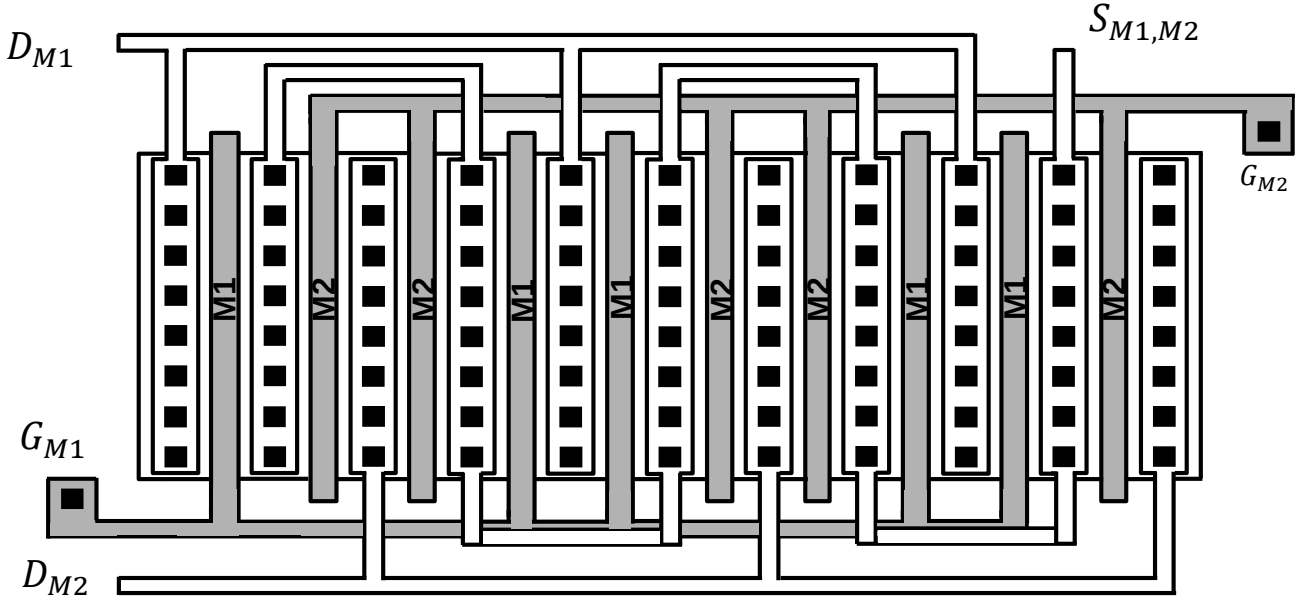


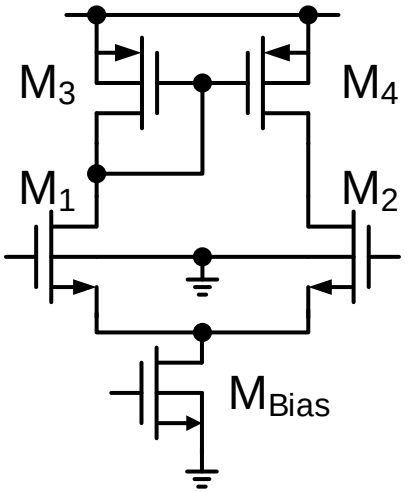
1st + 2nd order
Gradient mismatch model



Transistor Layouts

- Common-centroid layout for better matching accuracy
- Example: A differential source-coupled pair

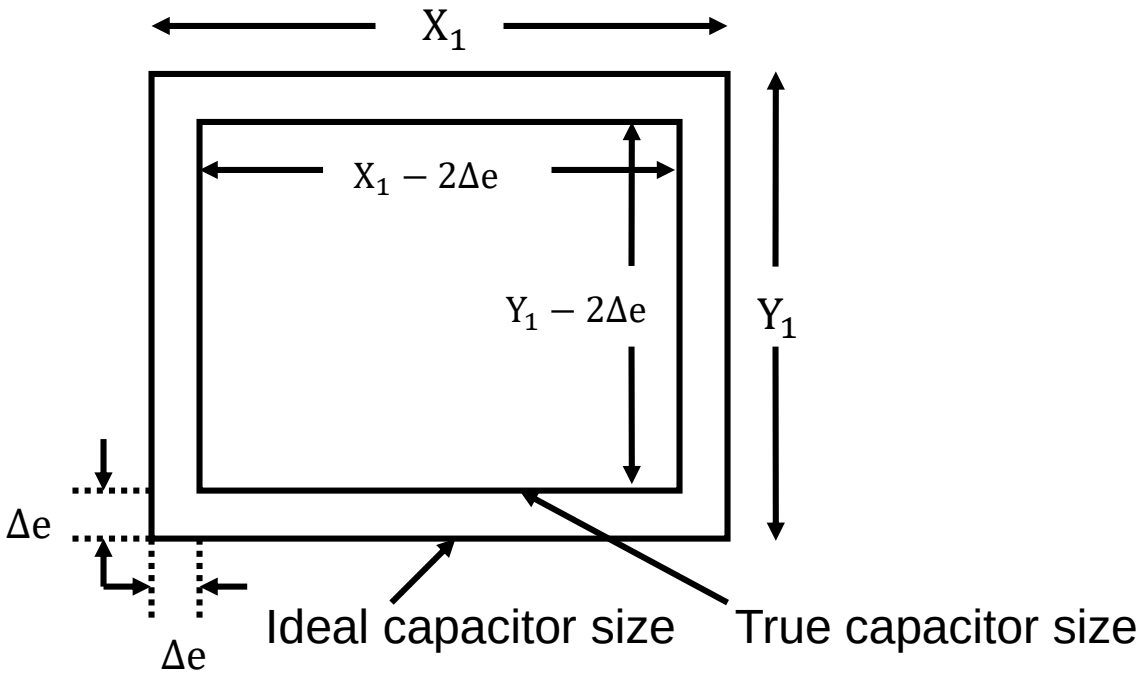




- The layout for M_1 and M_2 is symmetric in both the X and Y axes, and any gradients would affect both M_1 and M_2 in the same way
- This layout technique greatly minimize nonidealities such as OPAMP input-offset voltage errors when using a differential pair (M_1/M_2, M_3/M_4) in the input stage of an OPAMP

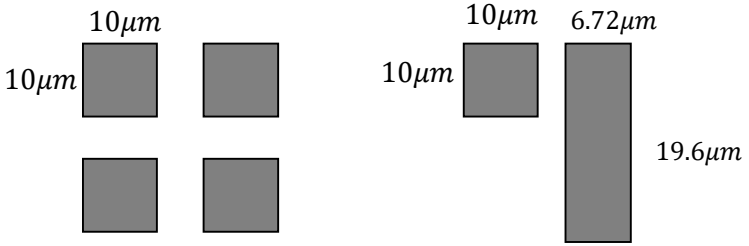
Capacitor Matching

- Two major sources of match errors are due to
  - Oxide-thickness gradient
    - Common-centroid layout can be used to minimize this error
  - Over-etching
    - Capacitor area is smaller than mask area

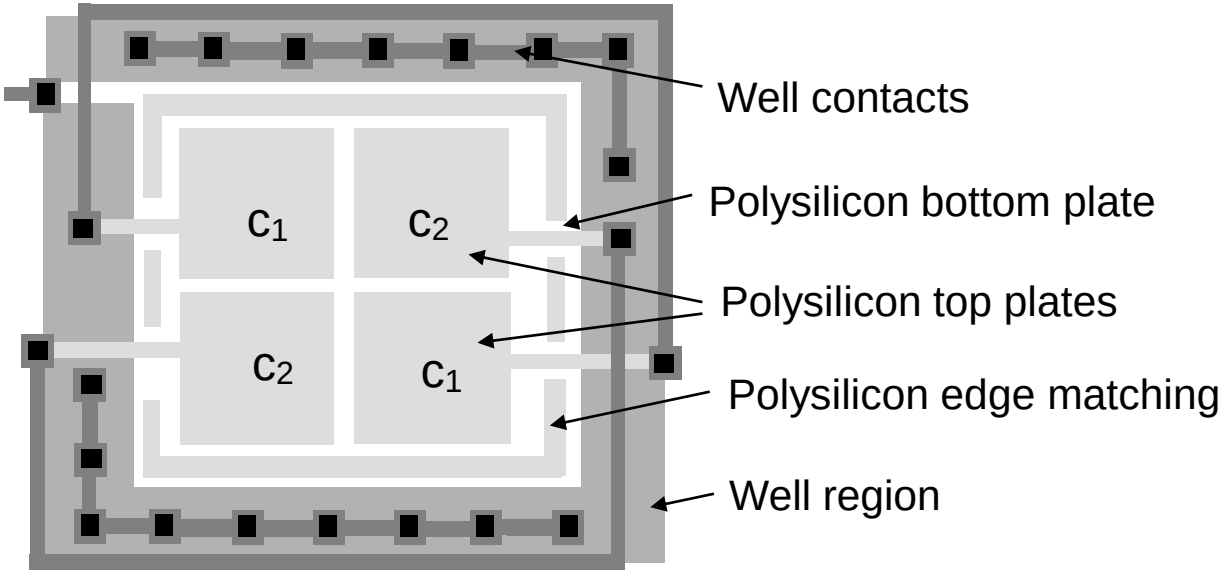


Capacitor Matching (Cont.)

- Error can be minimized
  - Use unit-sized capacitor
  - Perimeter-to-area ratios are kept the same, even where the capacitors are different sizes (Refer to p.104~106 of textbook).
    e.g. A capacitor layout with equal perimeter-to-area ratios of 4 units and 2.314units

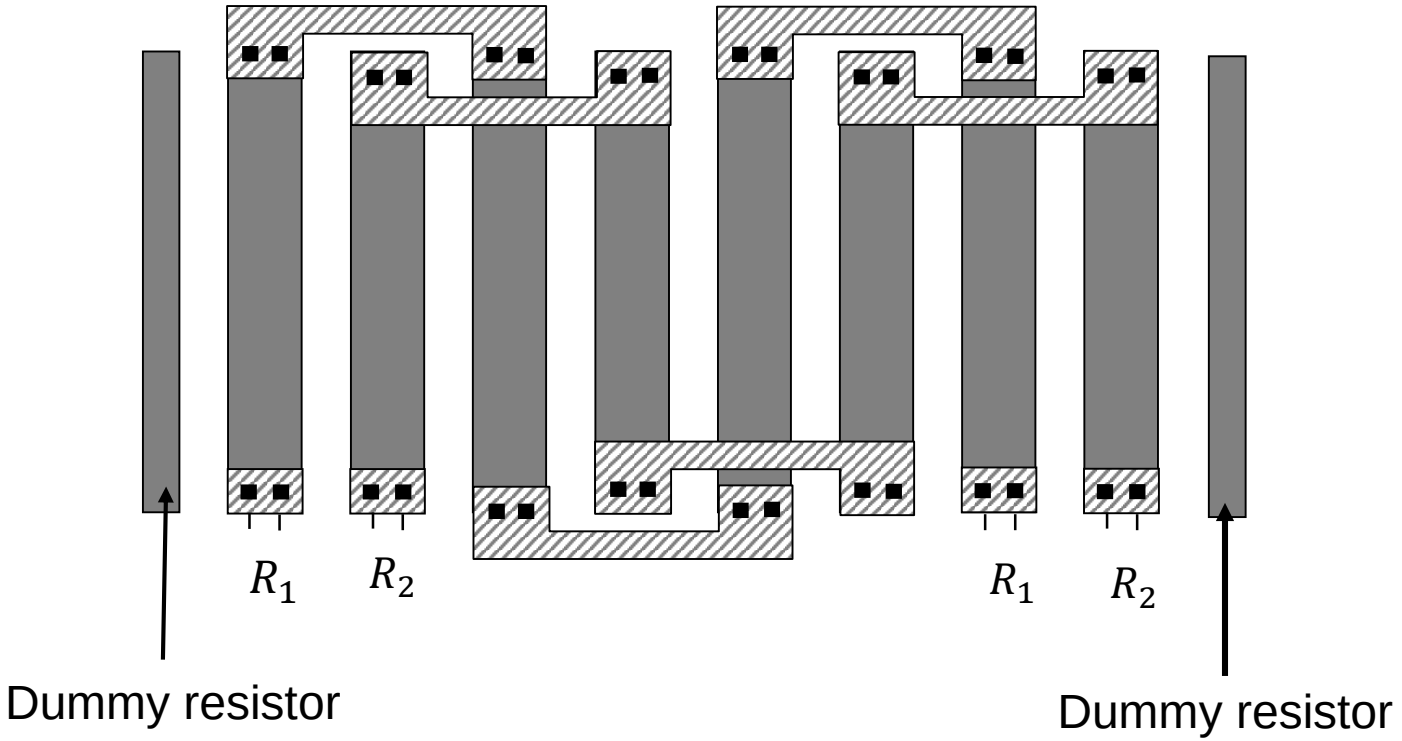


- To minimize 2nd-order effect (Refer to p.106~107 of textbook)



Resistor Matching

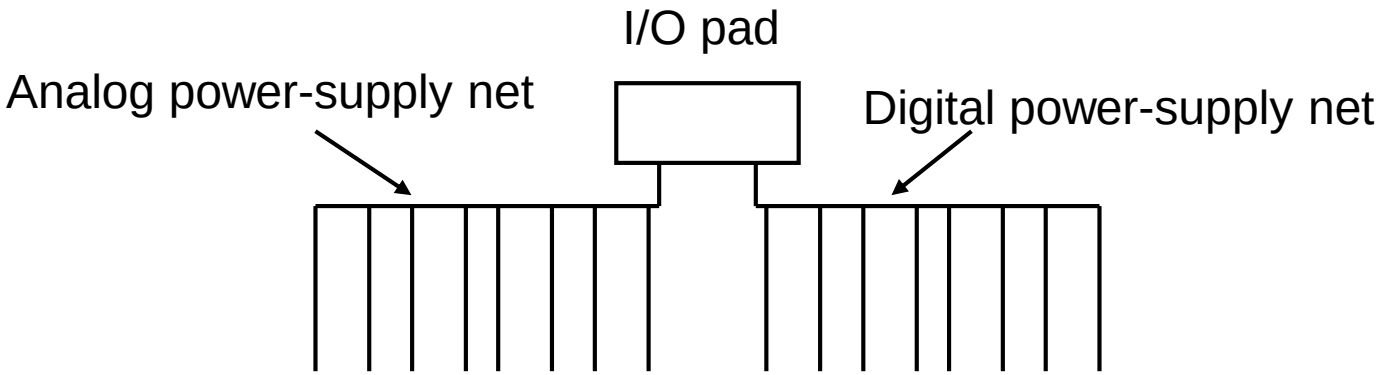
- The structure below might result in about 0.1% matching accuracy of identical resistors if the finger widths are relatively wide (say, 3μm in a 28nm technology)



Noise Considerations in Analog Layout

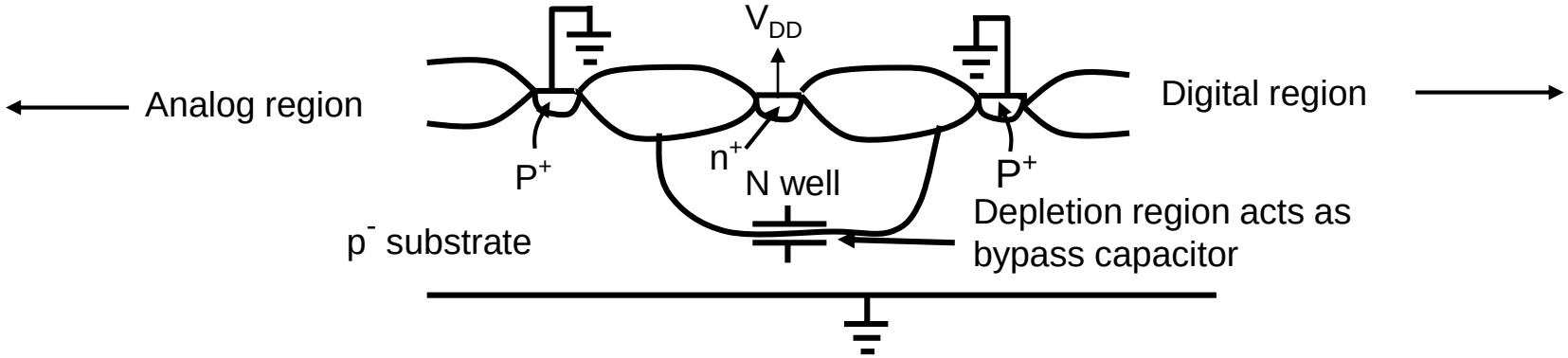
- Minimize noise in analog circuits
  - Minimize noise from digital circuits coupling into substrate or analog power supplies
  - Minimize substrate noise that affects analog circuits

- Example of noise reduction technique (Refer to p.109~112 of textbook)
  - Use separate nets for analog and digital power supplies

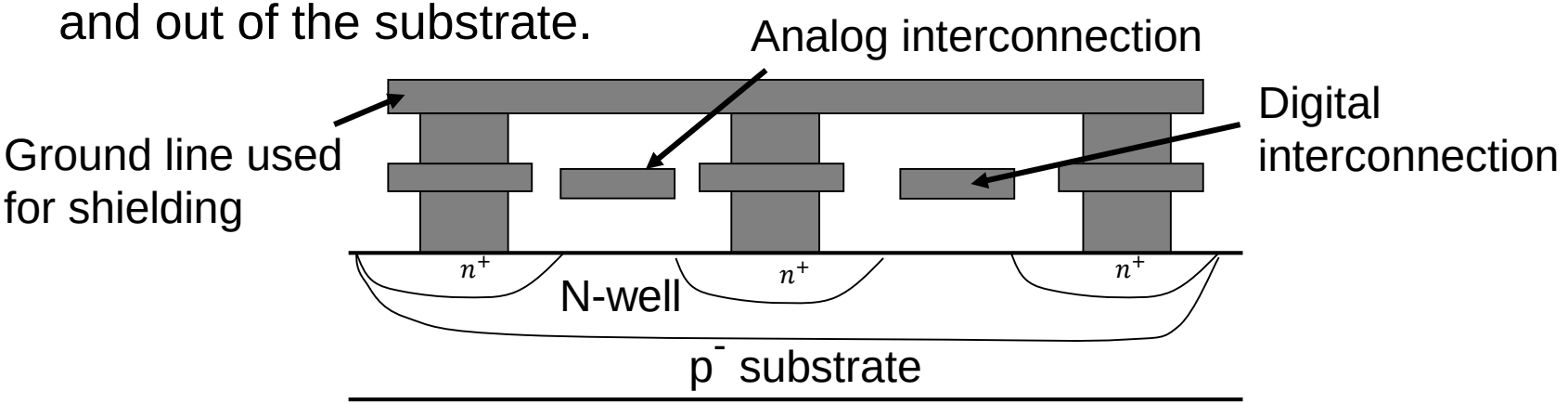


Noise Considerations in Analog Layout (Cont.)

- Examples of noise reduction technique (Cont.)
  - Separating analog and digital areas with guard rings and wells in an attempt to minimize the injection of noise from digital circuits into the substrate under the analog circuit.



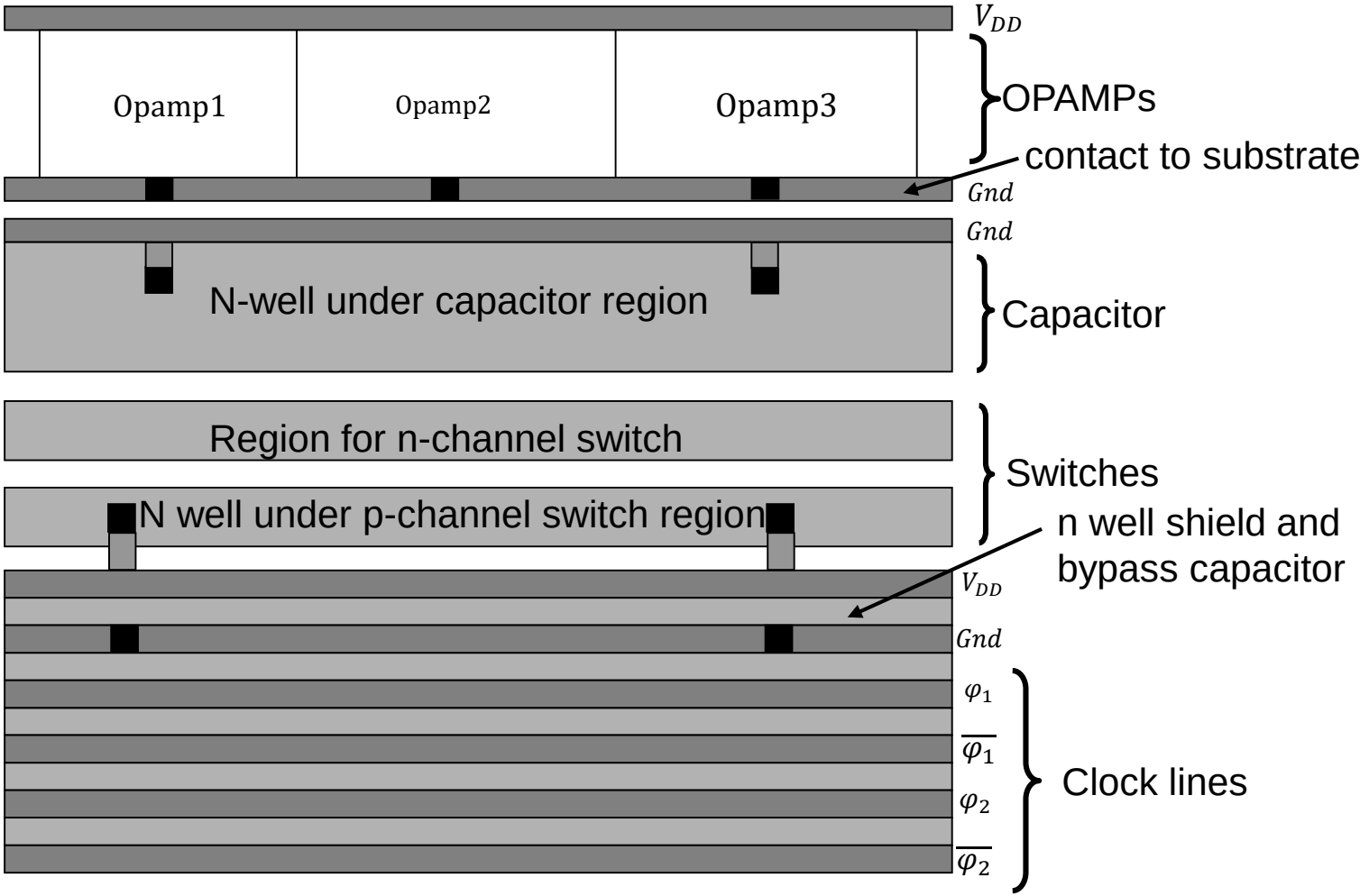
  - Using shields helps keep noise from being capacitively coupled into and out of the substrate.



Noise Considerations in Analog Layout (Cont.)

- Any unused space should be filled with additional contacts to both the substrate and to the wells, which are used as bypass capacitors.

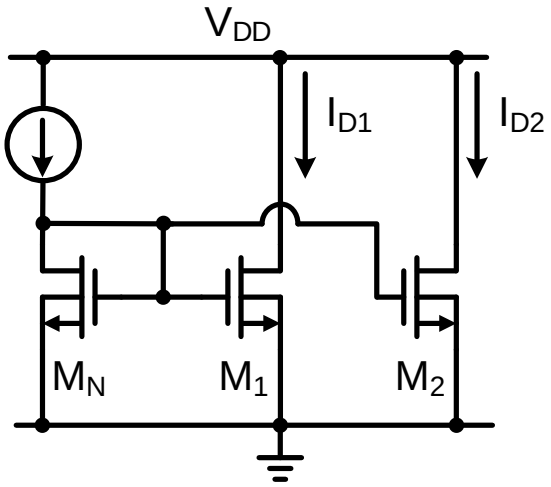
- A possible floorplan for an analog section containing switched-capacitor circuits.



Mismatch Effects in MOSFET Current Mirrors

- Mismatch between M1 and M2: W/L ratio & Threshold voltage
- Mathematical expression
  - Drain currents of M1 and M2

$$I_{D1}=\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1(V_{GS}-V_{t1})^2, I_{D2}=\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2(V_{GS}-V_{t2})^2$$



  - Define average and mismatch quantities

$$I_D=\frac{I_{D1}+I_{D2}}{2}, \Delta I_D=I_{D1}-I_{D2} \qquad V_t=\frac{V_{t1}+V_{t2}}{2}, \Delta V_t=V_{t1}-V_{t2}$$

$$\frac{W}{L}=\frac{1}{2}\left[\left(\frac{W}{L}\right)_1+\left(\frac{W}{L}\right)_2\right], \Delta\frac{W}{L}=\left(\frac{W}{L}\right)_1-\left(\frac{W}{L}\right)_2$$

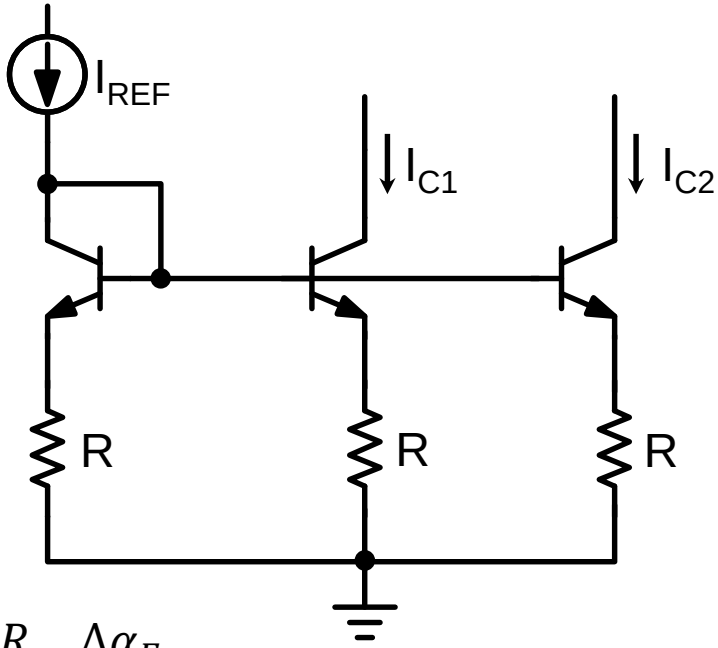
  - Substitute these expressions into I_{D1}, I_{D2} (Neglect high-order terms)

$$\frac{\Delta I_D}{I_D}=\frac{\frac{1}{2}\mu_n C_{ox}\left[\left(\frac{W}{L}+\frac{1}{2}\Delta\frac{W}{L}\right)\left(V_{GS}-V_t-\frac{1}{2}\Delta V_t\right)^2-\left(\frac{W}{L}-\frac{1}{2}\Delta\frac{W}{L}\right)\left(V_{GS}-V_t+\frac{1}{2}\Delta V_t\right)^2\right]}{\frac{1}{2}\times\frac{1}{2}\mu_n C_{ox}\left[\left(\frac{W}{L}+\frac{1}{2}\Delta\frac{W}{L}\right)\left(V_{GS}-V_t-\frac{1}{2}\Delta V_t\right)^2+\left(\frac{W}{L}-\frac{1}{2}\Delta\frac{W}{L}\right)\left(V_{GS}-V_t+\frac{1}{2}\Delta V_t\right)^2\right]}\cong\frac{\Delta\frac{W}{L}}{\frac{W}{L}}-\frac{2}{(V_{GS}-V_t)}\Delta V_t$$

    - Two mismatch components
      - Geometry dependent mismatch & Threshold voltage mismatch
    - I_D mismatch increases as (V_{GS}-V_t) is reduced

Mismatch Effects in BJT Current Mirrors

$$\frac{\Delta I_C}{I_C} = \left(\frac{1}{1+\frac{g_m R}{\alpha_F}}\right)\frac{\Delta I_S}{I_S} + \frac{\frac{g_m R}{\alpha_F}}{1+\frac{g_m R}{\alpha_F}}\left(-\frac{\Delta R}{R} + \frac{\Delta \alpha_F}{\alpha_F}\right)$$



- $g_m R >> 1$ => 2nd term dominates
- $g_m R << 1$ => 1st term dominates

- $g_m R >> 1$ is preferred because $\frac{\Delta I_s}{I_s} > \frac{\Delta R}{R} \& \frac{\Delta \alpha_F}{\alpha_F}$

Input Offset Voltage of Source-Coupled MOS Pair

- V_{os} : Differential voltage → Make differential output voltage exactly zero
- Define difference and average quantities

$$I_D = \frac{I_{D1} + I_{D2}}{2}, \Delta I_D = I_{D1} - I_{D2} \qquad R_L = \frac{R_{L1} + R_{L2}}{2}, \ \Delta R_L = R_{L1} - R_{L2}$$

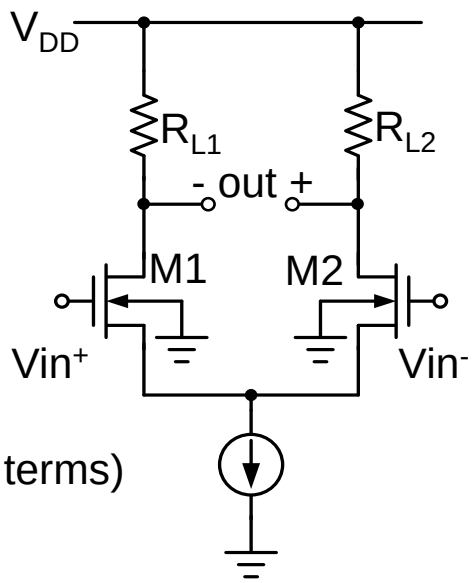
$$V_t = \frac{V_{t1} + V_{t2}}{2}, \ \Delta V_t = V_{t1} - V_{t2} \qquad \frac{W}{L} = \frac{1}{2}\left[\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2\right], \ \Delta\frac{W}{L} = \left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2$$

- Let $I_{D1}R_{L1} = I_{D2}R_{L2}$ → $\frac{\Delta I_D}{I_D} = \frac{-\Delta R_L}{R_L}$

$$V_{OS} = V_{GS1} - V_{GS2} = (V_{t1} + V_{ov1}) - (V_{t2} + V_{ov2})$$

$$= \Delta V_t + \sqrt{\frac{2}{u_n C_{ox}}}\left(\sqrt{\left(\frac{I_D + \frac{1}{2}\Delta I_D}{\frac{W}{L} + \frac{1}{2}\Delta\frac{W}{L}}\right)} - \sqrt{\left(\frac{I_D - \frac{1}{2}\Delta I_D}{\frac{W}{L} - \frac{1}{2}\Delta\frac{W}{L}}\right)}\right)$$

$$\cong \Delta V_t + \frac{(V_{GS} - V_t)}{2}\left[\left(\frac{-\Delta R_L}{R_L}\right) - \left(\frac{\Delta(W/L)}{(W/L)}\right)\right]$$ (Neglect higher order terms)



  - Mismatch components
    - Threshold voltage mismatch
    - Geometry dependent mismatch → Increase as (V_{GS}-V_t) is increased
- For same level of geometric mismatch or process gradient: V_{os}(MOSFET) > V_{os}(BJT)

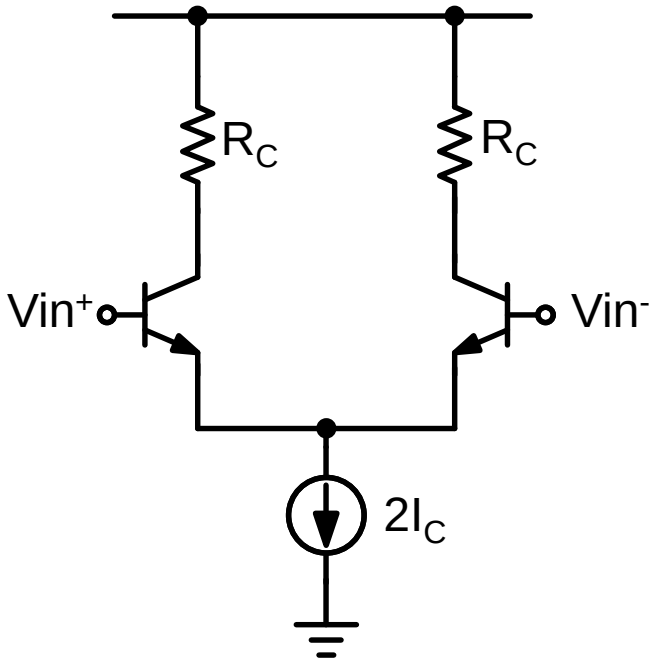
Input Offset Voltage of Emitter-Couple BJT Pair

- Offset voltage with resistor load

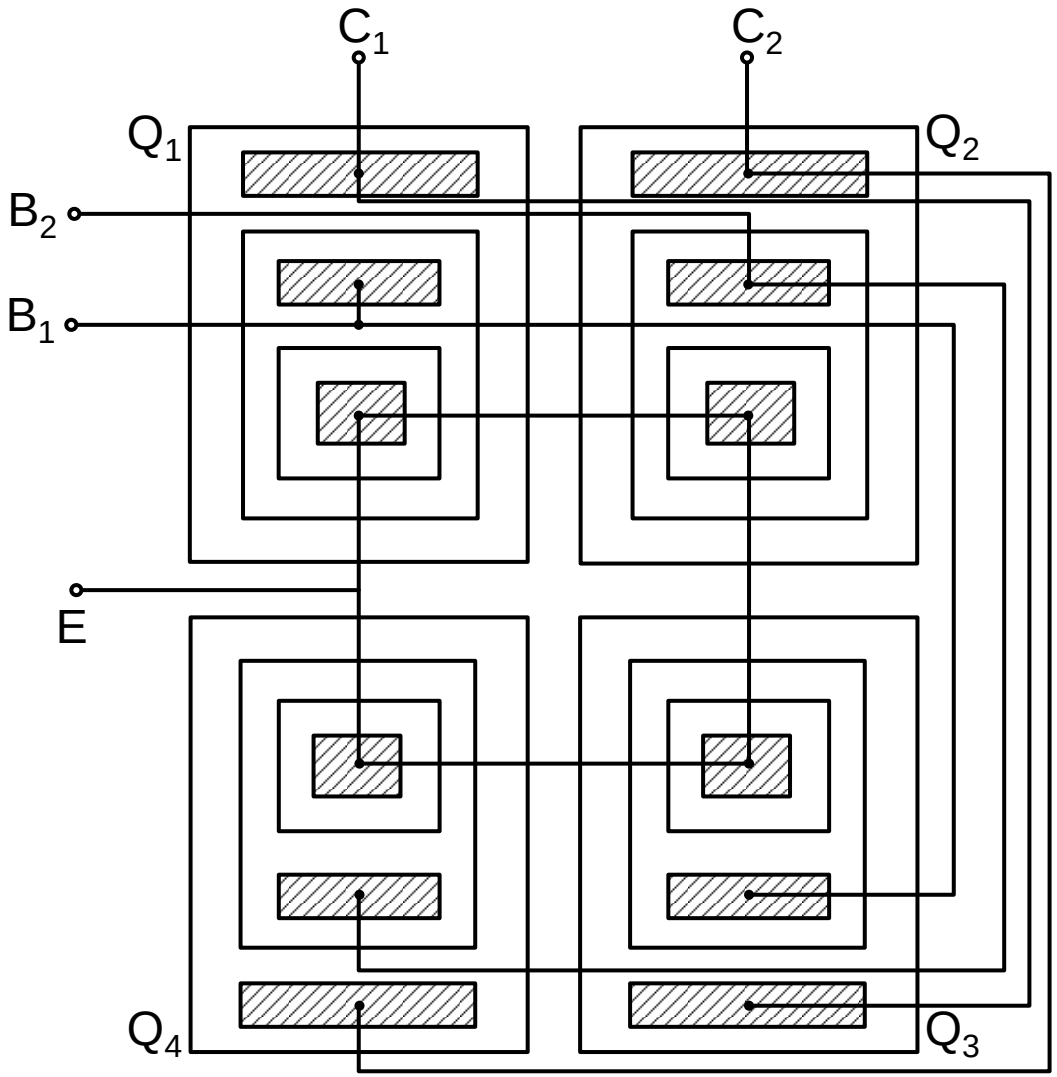
$$V_{os} \approx V_T\left(-\frac{\Delta R_c}{R_c} - \frac{\Delta I_s}{I_s}\right); \qquad \frac{dV_{os}}{dT} = \frac{V_{os}}{T}$$

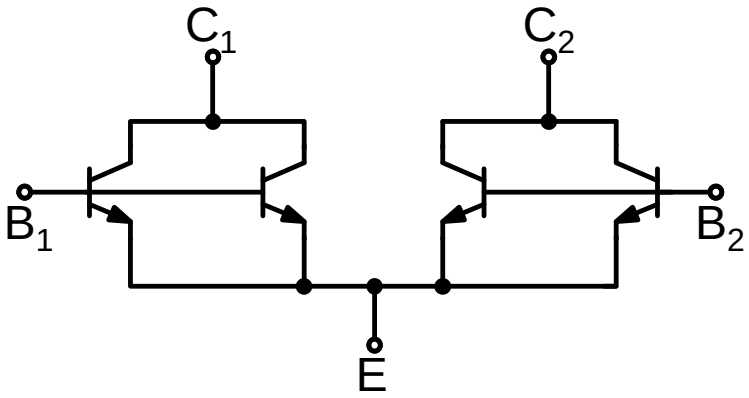
- Offset current with resistor load

$$I_{os} \approx -\frac{I_c}{\beta_F}\frac{\Delta R_c}{R_c} - \frac{I_c}{\beta_F}\frac{\Delta \beta_F}{\beta_F}$$



Common-Centroid Layout of BJT Pair





Input Offset Voltage of MOS OPAMP

- Assume that the matching is perfect with inputs grounded

$$V_{OUT} = V_{DD} - |V_{GS3}| \ldots (1)$$

- Differential input required to drive the output to the value given by (1) is the input-referred offset voltage. With device mismatch, offset is usually nonzero.

$$V_{ID} = V_{GS1} - V_{GS2} = V_{t1} + V_{ov1} - V_{t2} - V_{ov2} \ldots (2)$$

- Assume that λ of M_1 & M_2 are identical ($V_{DS1} = V_{DS2} = V_{DSN}$ when $V_{ID} = V_{OS}$)

$$V_{OS} = V_{t1} - V_{t2} + \sqrt{\frac{1}{1+\lambda_N V_{DSN}}}\left(\sqrt{\frac{2I_1}{k'(W/L)_1}} - \sqrt{\frac{2I_2}{k'(W/L)_2}}\right) \ldots (3)$$

- Assume that the mismatches are small

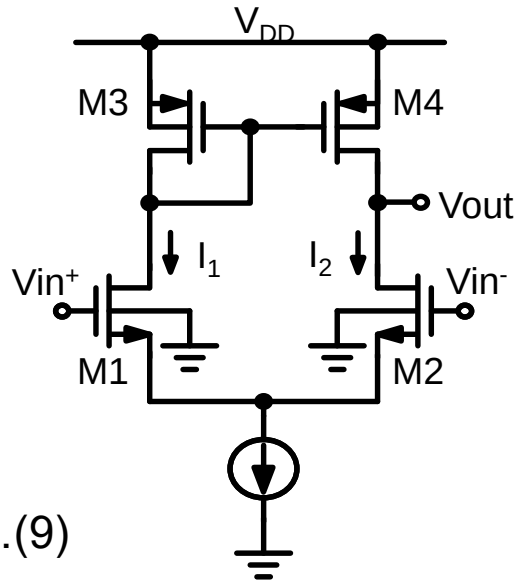
$$V_{OS} \approx V_{t1} - V_{t2} + \frac{V_{ovN}}{2}\left(\frac{\Delta I_N}{I_N} - \frac{\Delta(W/L)_N}{(W/L)_N}\right) \ldots (4)$$

where

$$V_{ovN} = \sqrt{\frac{2I_N}{k'(W/L)_N(1+\lambda_N V_{DSN})}} \ldots (5)$$

$$\Delta I_N = I_1 - I_2 \ldots (6) \qquad I_N = \frac{I_1+I_2}{2} \ldots (7)$$

$$\Delta(W/L)_N = (W/L)_1 - (W/L)_2 \ldots (8) \qquad (W/L)_N = \frac{(W/L)_1+(W/L)_2}{2} \ldots (9)$$



Input Offset Voltage of MOS OPAMP (Cont.)

- Since $I_1 = -I_3$ & $I_2 = -I_4$, where

$$\frac{\Delta I_N}{I_N} = \frac{\Delta I_P}{I_P} \ldots (10) \qquad \Delta I_P = I_3 - I_4 \ldots (11) \qquad I_P = \frac{I_3 + I_4}{2} \ldots (12)$$

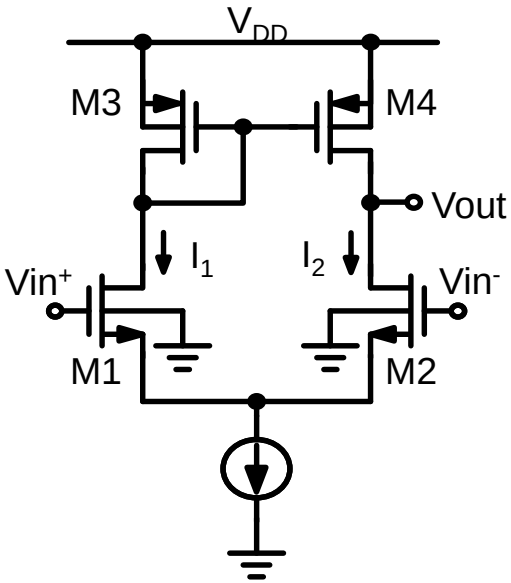
- Use KVL in the gate-source loop in the load to find $\Delta I_p / I_p$

$$0 = V_{GS3} - V_{GS4} = V_{t3} + V_{OV3} - V_{t4} - V_{OV4} \ldots (13)$$

- Since M3 and M4 are p-channel transistors, their overdrives are negative. Assume that the Early voltages of M3 and M4 are identical. Since $V_{DS3}=V_{DS4}=V_{DSP}$ when $V_{ID}=V_{OS}$, (13) can be rewritten as

$$0 = V_{t3} - V_{t4} - \sqrt{\frac{1}{1+|\lambda_P V_{DSP}|}}\left(\sqrt{\frac{2|I_3|}{k'(W/L)_3}} - \sqrt{\frac{2|I_4|}{k'(W/L)_4}}\right) \ldots (14)$$

- In (14), absolute value functions have been used
  - The arguments of the square-root functions are positive



Input Offset Voltage of MOS OPAMP (Cont.)

- If the mismatches are small, (14) can be approximated as

$$\frac{\Delta I_P}{I_P} \approx \frac{V_{t3}-V_{t4}}{|V_{ovP}|/2} + \frac{\Delta(W/L)_P}{(W/L)_P} \ldots (15)$$

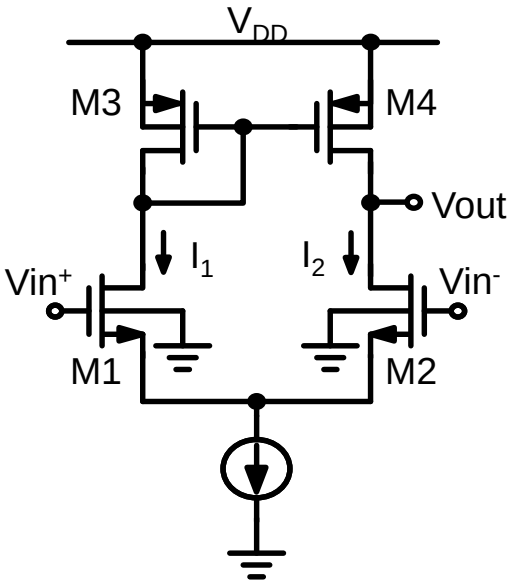
where $$|V_{OVP}| = \sqrt{\frac{2|I_P|}{k'(W/L)_P(1+|\lambda_P V_{DSP}|)}} \ldots (16)$$

$$\Delta(W/L)_P = (W/L)_3 - (W/L)_4 \ldots (17)$$

$$(W/L)_P = \frac{(W/L)_3+(W/L)_4}{2} \ldots (18)$$

- Substitute (15) and (10) into (4) gives

$$V_{OS} \approx V_{t1} - V_{t2} + \frac{V_{ovN}}{2}\left(\frac{V_{t3}-V_{t4}}{\frac{|V_{ovP}|}{2}} + \frac{\Delta(W/L)_P}{(W/L)_P} - \frac{\Delta(W/L)_N}{(W/L)_N}\right) \ldots (19)$$



Parameter Relevant for Transistor Performance

- T-like 0.18μm process

Parameter	Symbol	Typical value	Absolute accuracy	Matching accuracy
Threshold	V_{th}	0.45 V	$\pm 0.15\ V$	5 mV
Gamma	γ	0.3 ~ 0.6	-	-
Mobility (n)	μ_n	$250 cm^2/Vsec$	$\pm 10\%$	-
Mobility (p)	μ_p	$80 cm^2/Vsec$	$\pm 15\%$	-
Oxide capacitance	C_{ox}	$9 fF/\mu m^2$	-	-
Length	L	-	0.015 μm	-
Width	W	-	0.02 μm	-

Parameter Relevant for Capacitor Performance

- T-like 0.18μm process

Parameter	Symbol	Typical value	Absolute accuracy	Matching accuracy
Dielectric	$\varepsilon_{R(SiO_2)}$	3.9	-	-
Oxide thickness	t_{ox}	4.2 ± 0.2 nm	± 5%	-
Poly-oxide thick	$t_{p,ox}$	25 nm	-	-
MIM capacitor	C_{unit}	$6.1\ fF/\mu m^2$	-	0.4% on p-well 0.07% on n-well
VCC(PIP)	VCC	< 150 ppm	-	-
TCC(PIP)	TCC	< 50 ppm	-	-

Parameter Relevant for Resistor Performance

- T-like 0.18μm process

Parameter	Symbol	Typical value	Absolute accuracy	Matching accuracy
Diff. resistivity	ρ_{diff}	200 Ω/sq	25 %	2 %
Poly resistivity	ρ_{poly}	150 Ω/sq	20 %	4 %
Diff. thickness	$x_{j,diff}$	80 nm	15 %	0.5 %
Poly thickness	$x_{j,poly}$	80~100 nm	15 %	1 %